37 PIN CONNECTOR

CLOCK GEN BOARD AT: VME SLOT=4 DAC ADDR=8 SWITCH ADDR=2

PIN	NAME	CCD SIGNAL	CCD NUMBER	CODE	PIN	NAME
1	CLK0	PARALLEL 1	1	–	20	+12V
2	CLK1	PARALLEL 2	1	–	21	–12V
3	CLK2	PARALLEL 3	1	–	22	GND
4	CLK3	SUMMING WELL (A)	1	–	23	GND
5	CLK4	SERIAL PHASE #1 (A)	1	–	24	GND
6	CLK5	SERIAL PHASE #2 (A)	1	–	25	GND
7	CLK6	SERIAL PHASE #3	1	–	26	GND
8	CLK7	SERIAL PHASE #2 (B)	1	–	27	GND
9	CLK8	SERIAL PHASE #1 (B)	1	–	28	GND
10	CLK9	SUMMING WELL (B)	1	–	29	GND
11	CLK10	RESET GATE (A)	1	–	30	GND
12	CLK11	RESET GATE (B)	1	–	31	GND
13	CLK12	PARALLEL 1	2	–	32	GND
14	CLK13	PARALLEL 2	2	–		
15	CLK14	PARALLEL 3	2	–		
16	CLK15	SUMMING WELL (A)	2	–		
17	CLK16	SERIAL PHASE #1 (A)	2	–		
18	CLK17	SERIAL PHASE #2 (A)	2	–		
19	CLK18	SERIAL PHASE #3	2	–		
33	CLK19	SERIAL PHASE #2 (B)	2	–		
34	CLK20	SERIAL PHASE #1 (B)	2	–		
35	CLK21	SUMMING WELL (B)	2	–		
36	CLK22	RESET GATE (A)	2	–		
37	CLK23	RESET GATE (R)	2	–		

REVISION

01–08–97 CHANGED TITLES FROM PFCAM TO SDSU CCD CONTROLLER
03–05–97 REV. B – CHANGED SIGNAL NAMES TO REFLECT SDSU AND UCOLICK USAGE
11–23–98 REMOVED VIDEO LABELS
01–25–00 CHANGED FROM SDSU1 TO SDSU2

UNIVERSITY OF CALIFORNIA
LICK OBSERVATORY

PIN ASSIGNMENTS
CLOCK BOARD OUTPUT CONNECTORS
SDSU2 CCD CONTROLLER

DES'N BY: B. Alcott
ORIGIN DATE: 4/1/96
DRAWN BY:
MODIFY DATE: 01–25–00
PATH: ESI\SDSUCCD2\CLOCKCON
REV. C

DWG. NO. EL–3271–1D
NUM. 1 OF 1